Amendments to the Claims:

This Listing of Claims will replace all prior versions and listings of claims in the Application:

1. (Currently Amended) A semiconductor device comprising:

a substrate;

a gate region on top of the substrate;

a ~~first and second~~ sidewall liner ~~liners~~ situated on a ~~first and second sides~~ side of the gate region ~~respectively, the first and second sidewall liners~~ and having a vertical part contacting a sidewall ~~sidewalls~~ of the gate region and a horizontal part contacting the substrate; and

a ~~first and second~~ recessed ~~spacers~~ spacer situated on top of the ~~first and second~~ sidewall ~~liners respectively~~ liner,

wherein a height of the ~~first and second~~ recessed ~~spacers~~ spacer is lower than a height of the sidewall liner, ~~and~~

wherein the horizontal part of ~~each~~ the sidewall liner is shorter than the corresponding recessed spacer on top thereof; and

a contact etch stopping (CES) layer formed over the recessed spacer and having a predetermined stress level being one of compressive and tensile.

2. (Original) The device of claim 1 wherein the height of the recessed spacer is at least 50 Å lower than the height of the vertical part of the sidewall liner.

3. (Currently Amended) The device of claim 1 wherein the horizontal part of each gate sidewall liner is at least 10 Å shorter than the recessed spacer ~~spacers~~.

4. (Original) The device of claim 1 wherein the gate region further includes a gate dielectric and electrode layers.

5. (Original) The device of claim 4 wherein the height of the gate region does not exceed 1800Å.

6. (Original) The device of claim 1 wherein the recessed spacer is SiN based.

7. (Original) The device of claim 1 wherein the recessed spacer further includes Ge, Ar, or O_2 based impurities.

8. (Original) The device of claim 1 wherein the sidewall liner is oxide based.

9. (Cancelled)

10. (Currently Amended) The device of claim [[9]] 1 wherein the CES layer imposes a compressive stress.

11. (Currently Amended) The device of claim [[9]] 1 wherein the CES layer imposes a tensile stress.

12. (Currently Amended) The device of claim [[9]] 1 wherein the stress level of contact etching stopper layer is larger than 200M Pa.

13. (Original) The device of claim 9 wherein the thickness of the CES layer is smaller than 600Å.

14. (Withdrawn - Currently Amended) A method for fabricating at least one semiconductor device having a gate region and recessed spacers, comprising:

forming a substrate;

forming a gate region on top of the substrate, the gate region having a gate electrode and a gate dielectric region;

forming ~~two~~ a sidewall liner along a side of ~~liners confining~~ the gate region ~~therebetween~~;

forming a ~~two spacers~~ spacer on top of the sidewall ~~liners~~ liner ~~on both sides of the gate region~~, a height of the ~~spacers~~ spacer matching substantially a height of the sidewall ~~spacers~~ liner;

reducing the width of the sidewall ~~liners~~ liner underneath the ~~spacers~~ spacer to pull back from an edge of each spacer by a predetermined distance; and

forming ~~two~~ a recessed ~~spacers~~ spacer by reducing the height of the formed ~~spacers~~ spacer, wherein the reduced spacer height reduces device channel stress.

15. (Withdrawn - Currently Amended) The method of claim 14 wherein the forming ~~two spacers~~ a spacer further includes depositing spacer material and etching the deposited spacer material so that the top of the spacer slopes ~~spacers slope~~ down from the top of the sidewall ~~liners~~ liner to a horizontal part of the sidewall liner that extends along the substrate from the gate region.

16. (Withdrawn - Currently Amended) The method of claim 14 wherein the reducing further includes:

forming an oxide layer over the spacer ~~spacers~~, the sidewall liner ~~liners~~, and the gate region;

etching the oxide off within a predetermined time period so that the width of the sidewall liner is ~~liners are~~ pulled back for a predetermined distance.

17. (Withdrawn - Currently Amended) The method of claim 14 wherein forming ~~two~~ the recessed spacer ~~spacers~~ further includes selectively etching the ~~spacers~~ spacer to reduce at least 50Å in the height of the spacer ~~spacers~~ to form the recessed spacer ~~spacers~~.

18. (Withdrawn - Currently Amended) The method of claim 14 further comprising introducing one or more impurities to the ~~spacers~~ spacer to further reduce the device channel stress.

19. (Withdrawn - Currently Amended) The method of claim 14 wherein the predetermined distance pulled back from the edge of ~~each~~ the spacer is at least 10Å.

20. (Withdrawn - Currently Amended) The method of claim 14 further comprising forming a contact etch stopper (CES) layer over the recessed spacer ~~spacers~~ for further modifying the device channel stress.

21. (Withdrawn) The method of claim 20 wherein the CES layer imposes a compressive stress.

22. (Withdrawn) The method of claim 20 wherein the CES layer imposes a tensile stress.

23. (Withdrawn - Currently Amended) A transistor comprising:

a substrate;

a gate electrode on top of the substrate;

~~a first and second~~ an "L" shaped gate sidewall ~~liners confining~~ liner along the gate electrode and ~~therebetween, the first and second sidewall liners~~ having a vertical part contacting ~~sidewalls~~ a sidewall of the gate electrode and a horizontal part contacting the substrate; and

a ~~first and second~~ recessed spacer ~~spacers~~ situated on top of the ~~first and second~~ sidewall liner ~~liners respectively~~; and

a contact etching stopper (CES) layer situated over the recessed spacer ~~spacers~~,

wherein a height of the spacer ~~first and second spacers~~ is lower than a height of the gate sidewall liner ~~liners~~ and a width of the gate sidewall liner ~~liners~~ is shorter than that of the spacer ~~first and second spacers~~, and

wherein the recessed ~~spacers are~~ spacer is doped with predetermined impurities for modifying a channel stress of the transistor.

24. (Withdrawn - Currently Amended) The transistor of claim 23 wherein the recessed ~~spacers are~~ spacer is at least 50 Å lower than the gate sidewall liner ~~liners~~.

25. (Withdrawn - Currently Amended) The transistor of claim 23 wherein the gate sidewall ~~liners are~~ liner is at least 10Å shorter than the recessed spacer ~~spacers~~.

26. (Withdrawn - Currently Amended) The transistor of claim 23 wherein the impurities doped into the recessed spacer ~~spacers~~ includes Ge, Ar, or O_2 based impurities.

27. (Withdrawn - Currently Amended) The transistor of claim 23 wherein the CES layer formed over the recessed spacers is thicker than the recessed spacer ~~spacers~~.

28. (Withdrawn) The transistor of claim 23 wherein the contact etching stopper layer is thinner than 600Å.

29. (Withdrawn) The transistor of claim 23 wherein the contact etching stopper layer imposes a tensile stress less than 1.5G Pa.

30. (Withdrawn) The transistor of claim 23 wherein the contract etching stopper layer imposes a compressive stress less than 1.0G Pa.

31. (Withdrawn - Currently Amended) A semiconductor device comprising:

a substrate;

a gate region on top of the substrate;

~~two~~ a sidewall ~~liners~~ liner situated on at least one of two sides of the gate region; and

a spacer situated on top of each sidewall liner,

a contact etching stopper layer over each spacer ~~the spacers~~,

wherein the contact etching stopper layer is thicker than each ~~the~~ spacer.

32. (Withdrawn) The device of claim 31 wherein the thickness of contact etching stopper layer is smaller than 600Å.

33. (Withdrawn) The device of claim 31 wherein the contact etching stopper layer imposes tensile stress.

34. (Withdrawn) The device of claim 33 wherein a stress level of the contact etching stopper layer is less than 1.5G Pa.

35. (Withdrawn) The device of claim 31 wherein the contact etching stopper layer imposes compressive stress.

36. (Withdrawn) The device of claim 35 wherein a stress level of the contact etching stopper layer is less than 1.0G Pa.

37. (Withdrawn - Currently Amended) A semiconductor device comprising:

a substrate;.

a gate region on top of the substrate;

~~two~~ an "L" shaped sidewall liner ~~liners situated on~~ contacting each of two opposed [[sides]] sidewalls of the gate region;

a recessed spacer situated on top of each sidewall liner; and

a contact etching stopper layer formed over the spacers, the ~~sidewall~~ sidewalls, and the gate region,

wherein the contact etching stopper layer is thicker than the spacer, and

wherein the sidewall liner is higher and wider than the recessed spacer.

38. (Withdrawn) The device of claim 37 wherein the thickness of the contact etching stopper layer is smaller than 600Å.

39. (Withdrawn) The device of claim 37 wherein the contact etching stopper layer imposes a tensile stress.

40. (Withdrawn) The device of claim 39 wherein a stress imposed by the contact etching stopper layer is less than 1.5G Pa.

41. (Withdrawn) The device of claim 37 wherein the contact etching stopper layer imposes a compressive stress.

42. (Withdrawn) The device of claim 41 wherein a stress imposed by the contact etching stopper layer is less than 1.0G Pa.